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Automotive Semiconductor Device Suppliers Demonstrate Maturity in Driving Zero Defect Initiatives at Wafer Sort

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Today, electronic systems account for more than 20 percent of the value of a new automobile, and that figure is expected to increase to more than 40 percent by 2010[1]. The desire to increase reliability in this competitive marketplace, along with ensuring that safety liabilities are under control, have acted as significant catalysts for automotive device manufacturers to aggressively pursue “Zero Defect” semiconductor device manufacturing strategies.

1. Outlier Detection – The identification of quality risk devices within the passing devices population

“History has shown that parts with abnormal characteristics significantly contribute to quality and reliability problems.” This quote is taken directly out of the Automotive Electronics Council’s AEC-Q001 guideline, first published in 1997, which defined a concept for Part Average Testing (PAT). This was the first step in attempting to standardize a production strategy for identifying quality risk devices within the passing devices population. Semiconductor integrated device manufacturers supplying components to high reliability markets, such as the automotive industry, have been directly influenced to adopt PAT concepts for the identification and removal of device “Outliers” in the attempt to reduce Defective Parts Per Million (DPPM) rates.

Over the years, due to the lack of commercially available solutions, the semiconductor device supply base has pursued various methodologies consistent with PAT in order to identify and remove device quality risks during the manufacturing and test processes which simply fall short of being efficient, comprehensive, cost-effective or easy-to-implement within the production environment.

Leading edge sort processes, as represented in Figure 1 below, leverage all available sort test process data, enabling a post processing strategy that generates maximum outlier detection accuracy and coverage. This strategy not only facilitates the most comprehensive approach to performing Parametric Outlier detection strategies as discussed here, but enables a comprehensive implementation of sophisticated geographic or spatial analysis algorithms. The industry classic spatial analysis strategy is appropriately described as “Good Die in Bad Neighborhood”, where a tested good device is completely surrounded by test failures. Geographic algorithms may be extended to perform such strategies as test failure bin dependent proximity analysis and stepper pattern detections.

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[1] Source: *Joe Barkai of Manufacturing Insights, in his article - “Thinking Outside the (Auto) Box”, published online in Device Software Optimization, October 3, 2005.*

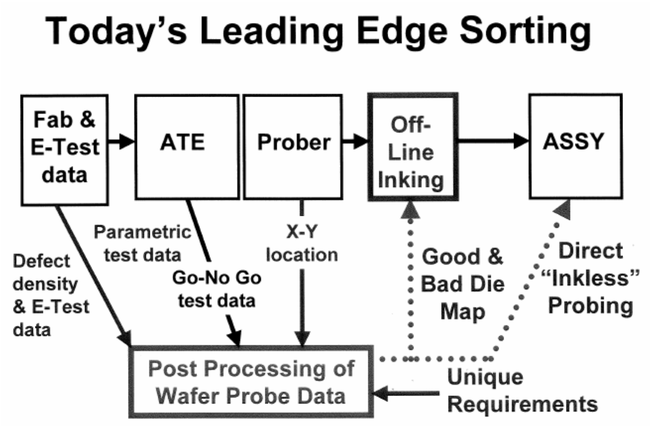


Figure 1: "Leading Edge" of Wafer Level Testing (as presented by Mann, William (2004) Chair, Southwest Test Workshop)

2. Parametric Outlier Detection for the Production Environment

When addressing the key attributes for an in-line post test data analysis tool, expectations are clear that this must be a robust, hands off, 24/7 solution that is fundamentally adaptive to the input data being analyzed. In order to achieve maximum outlier detection efficiency, any statistical analysis must comprehend a per-wafer, per-test solution, as it is recognized that each wafer represents a unique processing demographic as a result of modern wafer fabrication processing methodology. Outlier detection yield limit alarms generated as a result of classical outlier detection methodologies are a certain risk due to Wafer to Wafer process variances. These are symptoms that may also be manifested with the misclassification of good die as bad, or bad die as good. This may occur as a result of outlier identification scenarios that rely on sampling technologies driven by a limited sample size or, at the opposite extreme, too great a sample size taken across multiple wafer lots.

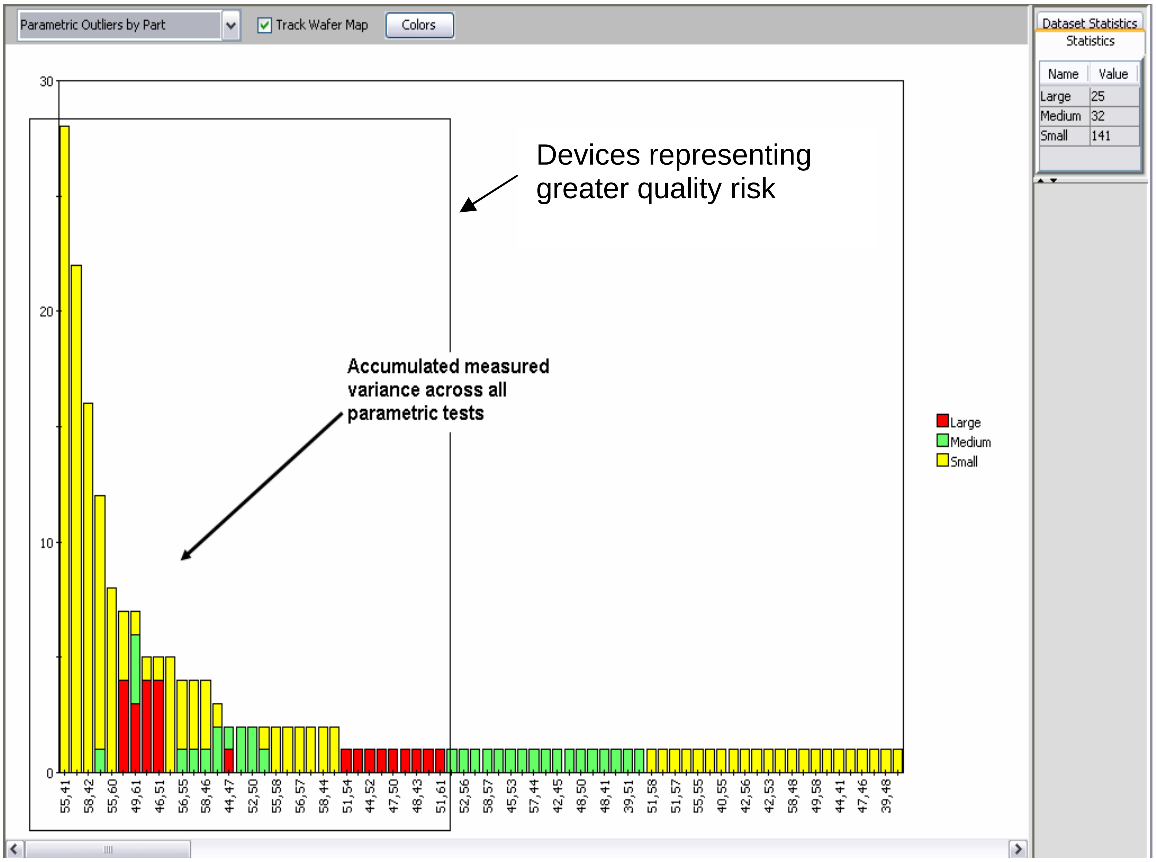
Recall that the fundamental principle of outlier detection is the identification of devices that are performing differently than the main population. The main population is best represented when it is specific to the wafer that is under analysis. For a complete parametric detection analysis, all parametric tests should be analyzed in order to identify a more accurate device quality classification.

3. Yield Improvement Opportunities

Device measured parametric variance is the key attribute that assigns the relative quality of a given device, in contrast to other devices sourced from the same wafer. The traditional PAT methodology focused on establishing what may be considered a more stringent "guard banding" approach, given this method only serves to establish tighter pass/fail control limits based solely on the statistics of the main population distribution for a given test. When required to catch more outliers, the user would simply tighten the control limit conditions, such as mean +/- 5 Sigma versus the PAT AEC suggestion of mean

+/- 6 Sigma. The result may or may not improve DPPM, but in fact it will significantly compromise yield by discarding additional good devices. As the PAT methodology has matured, it has become clear that more information is needed in order to make device quality risk decisions, thereby finding more quality risk devices without a significant impact to yield.

If we revisit the consideration of the magnitude of the variance for a specific device on a specific test, we may then look to how this device performed across multiple parametric tests by accumulating both the frequency and magnitude of these variances across all the tests. A representation of this strategy is displayed in Figure 2 below, with the Y-axis representing the number of occurrences for a given variance and the X-axis representing a specific die on the wafer.



Devices representing greater quality risk

Accumulated measured variance across all parametric tests

Dataset Statistics
Statistics

Name	Value
Large	25
Medium	32
Small	141

Figure 2: Accumulated Variance per Die Across All Parametric Tests

Despite the specific magnitude of variance for any given test, we find that the quality risk devices are identified by an accumulation of variance of differing magnitudes that occurred across all parametric tests. This additional data of both magnitude and frequency of occurrence generates a clear demographic of what devices are acting differently or are truly ‘abnormal’ in their respective behavior relative the main population. This methodology enables the next major DPPM improvement opportunity without the obvious compromise in yield associated with traditional guard banding strategies.

Given certain tests may be more significant indicators of correlated quality, we must also consider test weighting, as this may be critical to accurately establish a quality risk classification for a specific device. This methodology establishes a confidence in that the classification of accumulated variance magnitudes has identified accurately a quality risk device. Conversely, in that this action may accumulate *minimal* variances across multiple tests for other devices, we obtain a high confidence of quality for those respective devices. While traditional outlier detection methods are typically equated with yield loss, the opportunity to leverage this classification data as a feedback mechanism to revisit Statistical Bin Limit strategies at sort, offer a real potential to increase the overall manufacturing yield.

This advanced sort process achieves superior DPPM levels that the automotive industry is demanding while achieving improvements in overall manufacturing process yields, and therefore facilitating improved operating cost. This has been demonstrated by the additional fact that these methods are now aggressively being deployed across all product markets such as telecommunications and consumer, due to the attractive cost versus benefit tradeoff.